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# GLD2 Generic (JTAG) Linker Device

**Features**

- ATPG support in all major software vendor tools
- Functionally compatible with Lattice Semiconductor BSCAN2 reference design
- Small LUT count in programmable logic device
- High TCK rate achievable
- Customisation of functionality avalaible

**Overview**

The GLD2 provides 4 or more IEEE1149.1 (JTAG) ports that can be multiplexed to a single master port. By providing multiple local scan ports that can be omitted or included into the active scan chain the GLD2 provides the ability to symplify the JTAG architecture on the PCBA and reduce the test execution times.

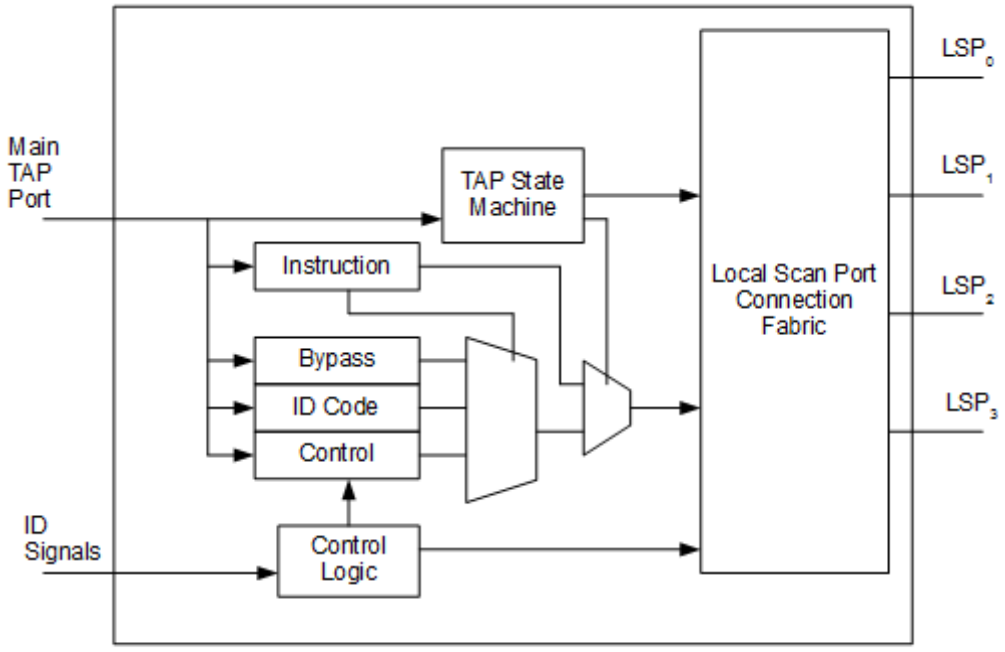



Figure : GLD2 Block diagram

**Pin Descriptions**

| Pin Name | Number Of Pins) | I/O | Description |
|---|---|---|---|
| TOEn | 1 | I | This signal, when low, causes all outputs on the device to be in the high impedance state. |
| TRSTn | 1 | I | This is the master Test Reset as described by IEEE1149.1. |
| TCK | 1 | I | This is the master Test Clock as described by IEEE1149.1. |
| TMS | 1 | I | This is the master Test Mode Select as described by IEEE1149.1. |
| TDI | 1 | I | This is the master Test Data In as described by IEEE1149.1. |
| TDO | 1 | O | This is the master Test Data Out as described by IEEE1149.1. |
| $ID_{(1 - 4)}$ | 4 | I | The 4 pins input value can be read by software via the IEEE1149.1 interface. |
| $LSP\_TRSTn_{(1 - 4)}$ | 4 | O | The Test Reset pin as defined by IEEE1149.1 for each of the LSPs. |
| $LSP\_TCK_{(1 - 4)}$ | 4 | O | The Test Clock pin as defined by IEEE1149.1 for each of the LSPs. |
| $LSP\_TMS_{(1 - 4)}$ | 4 | O | The Test Mode Select pin as defined by IEEE1149.1 for each of the LSPs. |
| $LSP\_TDI_{(1 - 4)}$ | 4 | I | The Test Data In pin as defined by IEEE1149.1 for each of the LSPs. |
| $LSP\_TDO_{(1 - 4)}$ | 4 | O | The Test Data Out pin as defined by IEEE1149.1 for each of the LSPs. |

### Functional Description

The GLD2 IP consists of the main IEEE1149.1 test access port (TAP) state machine which is closely coupled to the state machine for each local scan port control. There is the standard supporting logic for the TAP including the instruction register and bypass register along with the option logic to support the GLD2 functions which include the control register and the ID register. The selection loaded into the control register in conjunction with the local scan port state machine determines the inclusion or omission of an local scan port from the active scan chain.

The main state machine for the GLD2 is the IEEE1149.1 TAP access port the state diagram is show in the following figure.

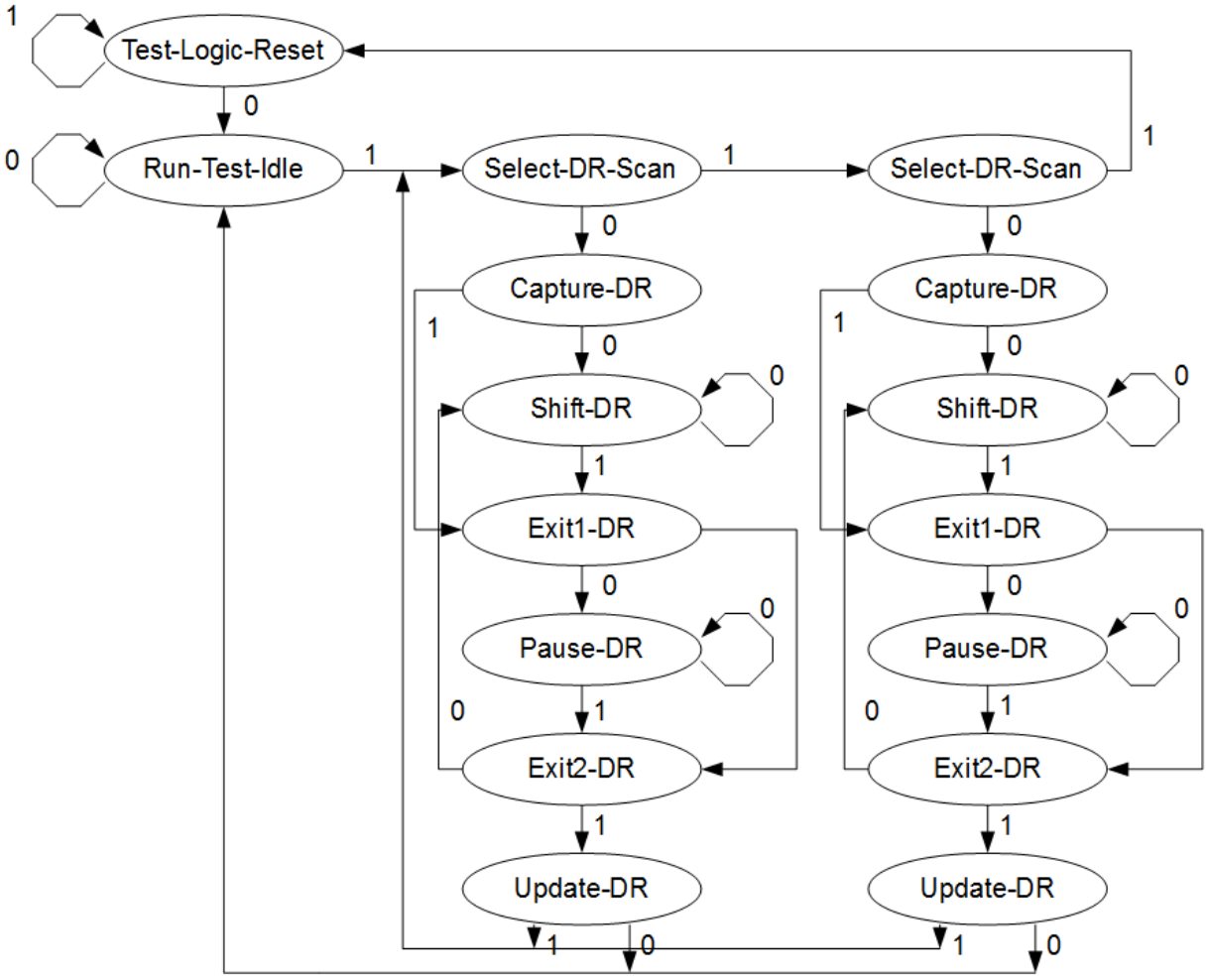



Figure : IEEE1149.1 Test Access Port State machine.

This TAP port controls the selection of the active data register for scan operations. The GLD2 supports 4 data registers which enables the selection of the active local scan port along with the reading if the device ID pins and providing the mandatory bypass register. The select register for the 4 local scan port inplementation is 8 bits in length. The size of the select register can be expanded to support implemnations of th GLD 2 supporting more than 4 local scan ports.

| Register Name | Register Size (Bits) | Description |
|---|---|---|
| Instruction Register | 8 | IEEE1149.1 required instruction decode register |
| Bypass Register | 1 | IEEE1149.1 required register |
| ID Register | 4 | Provides readable data that can be set on the I/O of the GLD2 |
| Select Register | 8 | Provides the control for the local scan ports in the GLD2 |

Figure : GLD2 Register Descriptions

| Instruction | Hex Op Code Value | Active Data Register |
|---|---|---|
| SCANIDB | FC | ID Register |
| READIDB | 7D | ID Register |
| SCANSEL | 7E | Select Register |
| BYPASS | *Unspecified values | Bypass Register |

*All Op code values not specified connect the Bypass register on the device

Table : GLD2 Instruction Operation Codes

**Instruction Descriptions**

**BYPASS** : Selects the BYPASS register to be connected into the active scan chain

**SCANIDB** : Selects the ID register to be connected into the active scan chain enabling the ID pins of the GLD2 to be read

**READIDB** : Selects the ID register to be connected into the active scan chain, the value of the ID pins on the device can not be read using this instruction

**SCANSEL** : Selects the Select register to be connected into the active scan chain, enabling the selection of local scan ports to be included in the active scan chain

## Register Descriptions

**INSTRUCTION REGISTER** : The IEEE1149.1 mandatory instruction register performs a method of selecting the active data register as per the IEEE1149.1 specification. The capture value of the instruction register is XXXXXX01 .

**BYPASS REGISTER** : The IEEE1149.1 mandatory bypass register on the GLD2 provides a single bit data path for the Shift-DR operation on the GLD2.

**ID REGISTER** : The ID register provides a method of reading the value presented on the ID pins of the device.

**SELECT REGISTER** : The SELECT register provides the control of the LSPs on the GLD2 each LSP can have its TMS signal held in a defined stable state or be included in the active scan chain.

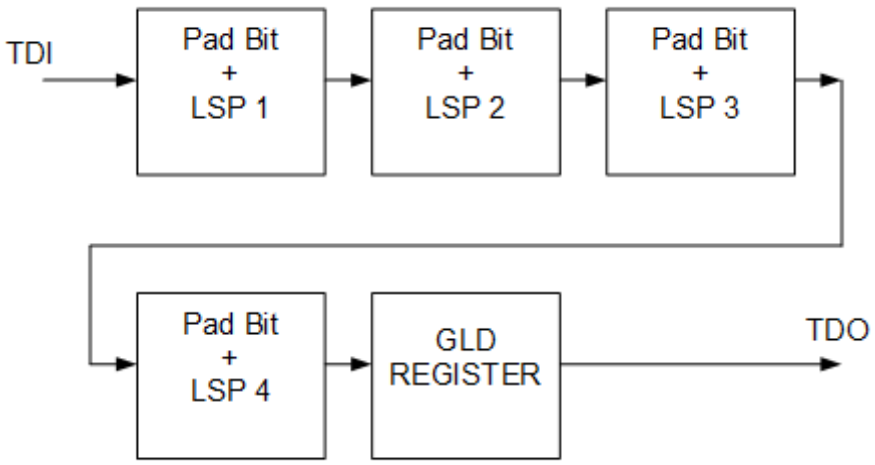
| Bit | Function |
|---|---|
| 0 | $TMS_1$ Stable State |
| 1 | Enable $LSP_1$ |
| 2 | $TMS_2$ Stable State |
| 3 | Enable $LSP_2$ |
| 4 | $TMS_3$ Stable State |

| | |
|---|---|
| 5 | Enable $LSP_3$ |
| 6 | $TMS_4$ Stable State |
| 7 | Enable $LSP_4$ |

Figure : Select register bit definitions

## Local Scan Port Connection Sequence

The LSPs can be included in the the active scan chain by the assocoated bit within the select register. The 8 bit select register supports 4 LSPs which can be connected as per the following diagram




Note : The GLD register is always preset independent on the presence of LSPs

Diagram : Local Scan Port Connection Sequence

## Increasing The Number of Local Scan Ports Supported

For designs that require more than 4 LSPs it is possible to support this requirement in two ways. The choice between the two methods will be driven by the test tool being used on the project.

**Cascade Mode**

The GLD2 many be cascaded to provide 8 LSPs. This method of expansion is used by the JTAG Technology's tool set. The logic for the GLD2 is implemented twice in order to provide the total of 8 LSPs. The active scan chain will have 2 sets of GLD registers present at all times.

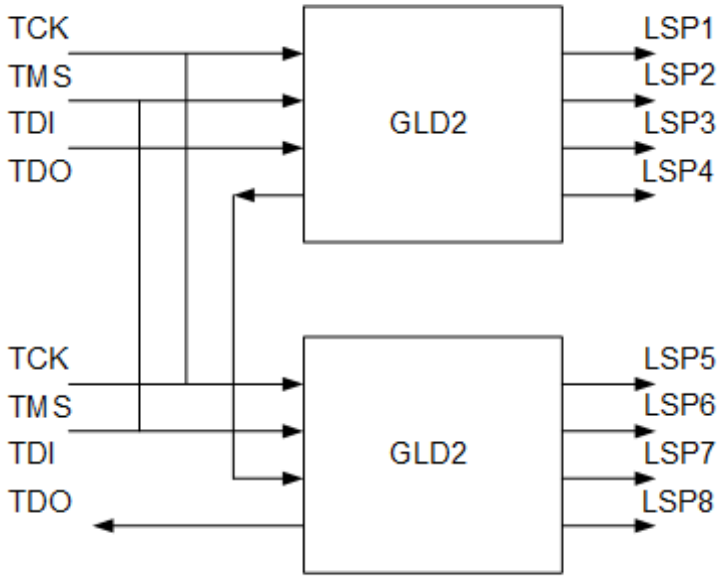



Figure : GLD2 Cascade operation

The LSPs are connected as shown in the following figure when all LSPs are active when used in the cascade mode. If no LSPs are active the active scan chain will contain the two applicable GLD registers.

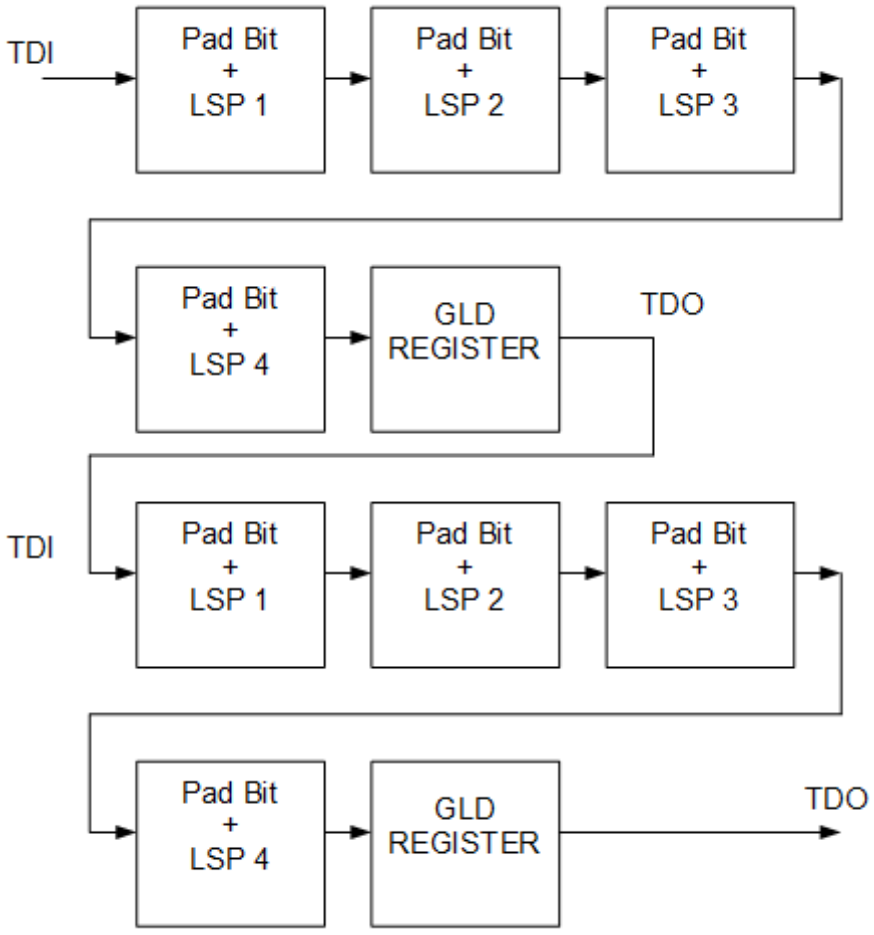


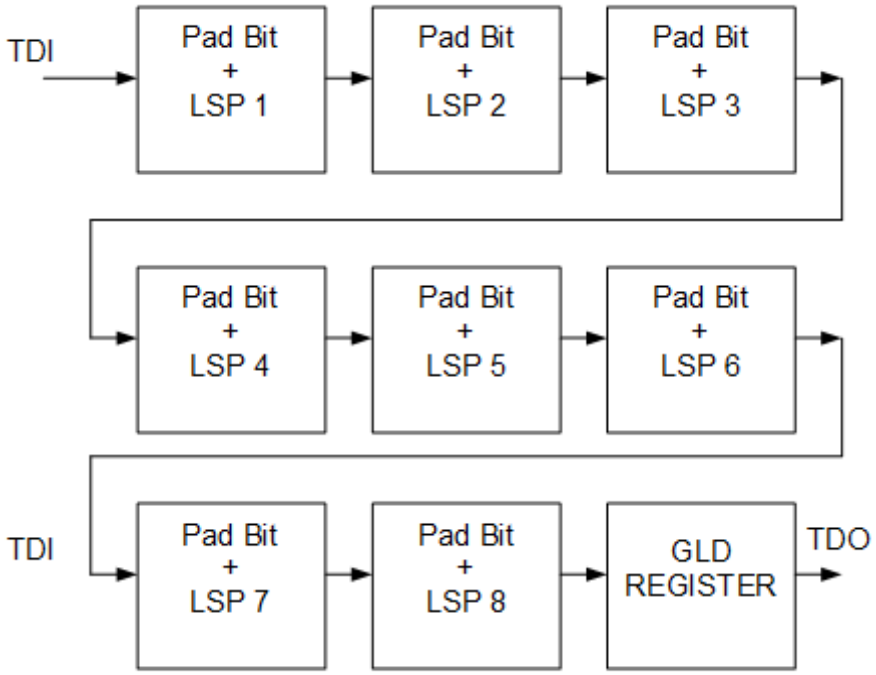

Figure : Cascade LSP connections

**Expanded Select register Mode**

The number of supported LSPs in the GLD may also be increased by the enlarging of the select register in the device. By increasing the select register by increments of 8 bits in size it is possible to support an additional 4 LSPs. If the select register is increased to 24 bits then the GLD2 supports an additional 4 LSPs givinga total of 12 LSPs and so on. The expanded select register solution is used with the Asset-Intertech and Corelis tool sets.

| Bit | Function |
|---|---|
| 0 | $TMS_1$ Stable State |
| 1 | Enable $LSP_1$ |
| 2 | $TMS_2$ Stable State |
| 3 | Enable $LSP_2$ |
| 4 | $TMS_3$ Stable State |
| 5 | Enable $LSP_3$ |
| 6 | $TMS_4$ Stable State |
| 7 | Enable $LSP_4$ |
| 8 | $TMS_5$ Stable State |
| 9 | Enable $LSP_5$ |
| 10 | $TMS_6$ Stable State |
| 11 | Enable $LSP_6$ |
| 12 | $TMS_7$ Stable State |
| 13 | Enable $LSP_7$ |
| 14 | $TMS_8$ Stable State |
| 15 | Enable $LSP_8$ |

Figure : Enlarged Select Register Support for 8 LSPs




Note : Any LSP may be omitted but the GLD2 register is always present in the scan chain

Figure : Expanded Select Register 8 LSP active scan chain connections

Also avaliable are expanded select register versions of a 12 and 16 port GLD device. For cascade implementations the GLD2 4port IP can be used to expand the LSP count to the desired LSP count. It should be note that the device utilisation and the maximum TCK rate performance using a cascade solution is beneficial compared to the expanded select register method.

## GLD2 Implementation

The GLD2 is currently supplied in multiple formats the first being NGO components for the Lattice Diamond tool providing a solution where the optimised IP can be integrated with customer logic in the target FPGA. To support the usage of the NGO flow implementation examples in both verilog and and VHDL are supplied. A Lattice edif file is also supplied this enables the GLD2 to be placed and routed stand alone in a selected FPGA device. Generic verilog code is also provided which allows the additional user logic to be intergrated with the GLD2 IP. The verilog code is generic and can be targeted to any vendors programmable device. This provides an FPGA vendor independent solution for JTAG scan chain management.

GLD2 : 4 Port Implementation

| Device | Speed Grade | Utilisation | $F_{max}$ (Mhz) | Number of I/Os |
|---|---|---|---|---|
| LCMX02-640HC-4TG100C | -4 | 78 LUTs | >30 | 30 |

GLD2 : 8 Port Implementation (Expanded Select Register )

| Device | Speed Grade | Utilisation | $F_{max}$ (Mhz) | Number of I/Os |
|---|---|---|---|---|
| LCMX02-640HC-4TG100C | -4 | 117 LUTs | >30 | 50 |

GLD2 : 8 Port Implementation (Cascade)

| Device | Speed Grade | Utilisation | $F_{max}$ (Mhz) | Number of I/Os |
|---|---|---|---|---|
| LCMX02-640HC-4TG100C | -4 | 131 LUTs | >30 | 50 |

Note :
In all bench marks the Lattice Diamond® 3.1 design software was used with default settings

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